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OFFICIAL**To:** Gautam Patel**From:** Brian Dutton**Fax:** 703-872-9306**Pages:** 9 + Coversheet**Phone:** 703-308-7940**Date:** May 21, 2004**Re:** Serial No.: 10/000,347**cc:**

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● **Comments: URGENT DUPLICATE AFTER FINAL RESPONSE**

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Inventor: Mamoru Kudo Atty Docket No.: SON-2274

Application No.: 10/000,347-Conf. #9724 Filing Date: December 4, 2001
Title: PHASE LOCKED LOOP CIRCUIT FOR REPRODUCING A CHANNEL CLOCK

Documents Filed:

Resubmission of Request for Reconsideration of Final Office Action (2 pages)

Copy of Request for Reconsideration of Final Office Action filed 2-13-04 (5 pages)
w/copy of date-stamped filing receipt indicating filing thereof

61

Docket No.: SON-2274
(80001-2274)

Application No.: 10/000,347
Mail Stop AF

AF-
2655



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Patent Application of

Mamoru KUDO et al.

Serial No.: 10/000,347

Filed: December 4, 2001

Confirmation No. 9724

Art Unit: 2655

Examiner: Gautam Patel

8/9/04
S/27/04
OK

For: PHASE-LOCKED LOOP CIRCUIT FOR REPRODUCING A CHANNEL CLOCK

RESUBMISSION OF
REQUEST FOR RECONSIDERATION OF FINAL OFFICE ACTION

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Sir:

A Request For Reconsideration Of Final Office Action was filed on February 13, 2004. A copy of the Request For Reconsideration Of Final Office Action, along with a copy of the postcard receipt, is provided herewith.

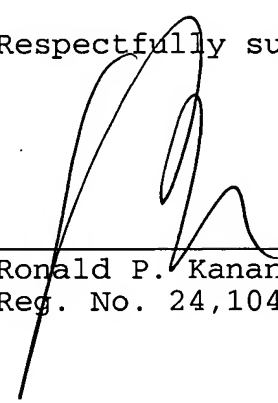
Acknowledgment and entry of the Request is respectfully requested.

Please take these documents into account in the examination of this application and make their consideration of record.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753 or the undersigned attorney at the below-listed number. If any fee is required, the Commissioner is hereby authorized to charge the fee to Deposit Account # 18-0013.

Respectfully submitted,

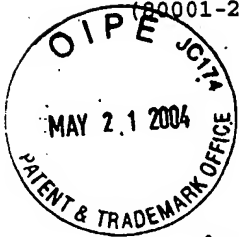
Date: May 21, 2004



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Patent Application of

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Serial No.: 10/000,347

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For: PHASE-LOCKED LOOP CIRCUIT FOR REPRODUCING A CHANNEL CLOCK

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Sir:

This is in full and timely response to the Final Office Action mailed on December 23, 2003. Reexamination in light of the following remarks is respectfully requested.

Claims 3-7 are currently pending in this application, with claim 3 being independent. No new matter has been added.

Rejections under 35 U.S.C. 112

Claims 3-7 were rejected under 35 U.S.C. 112, first and second paragraphs.

This rejection is traversed at least for the following

reasons. 35 U.S.C. §112 "requires only an objective enablement; the invention needs to be sufficiently disclosed through illustrative examples or terminology to teach those of ordinary skill in the art how to make and how to use the invention as broadly as it is claimed" (emphasis added). *Musco Corp. v. Qualite Inc.*, 41 USPQ2d 1954 (Fed. Cir. 1997). See also M.P.E.P §§2164.01, 2164.04.

In addition, "for claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims." *General Electric Co. v. Nintendo Co.*, 50 USPQ2d 1910, 1914 (Fed. Cir. 1999).

As shown at least within figures 2, 4 and other figures and descriptions throughout the specification, claim 3 and the claims dependent thereon include the features of:

a channel clock generation reference signal frequency divider 42 that divides a channel clock generation reference signal Vclk (page 20, lines 2-4);

a switching frequency divider 43 having a switch SW21, a first switching frequency divider 43a and a second switching frequency divider 43b (page 27, lines 8-12),

said first and second switching frequency dividers 43a,b receiving a high-frequency signal HIF (figure 4),

said first switching frequency divider 43a dividing said high-frequency signal HIF by a first dividing ratio to generate a first divided signal,

said second switching frequency divider 43b dividing said high-frequency signal by a second dividing ratio to generate a second divided signal,

said switch SW21 outputting said first divided signal during playback of a first recording medium and outputting said second divided signal during playback of a second recording medium (page 27, line 20 to page 28, line 6); and

a phase comparator 44, said phase comparator 44 receiving said divided channel clock generation reference signal and one of said first and second divided signals (page 27, lines 18-20),

said phase comparator 44 compares the phase of said divided channel clock generation reference signal with one of said first and second divided signals to output a phase error signal (page 20, lines 18-24).

No prior art has been cited against these claims. Thus, all claims are deemed allowable as a result. Withdrawal of the rejections and allowance of the claims is respectfully requested.

Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance. Accordingly, favorable reexamination and reconsideration of the application in light of the amendments and remarks is courteously solicited.

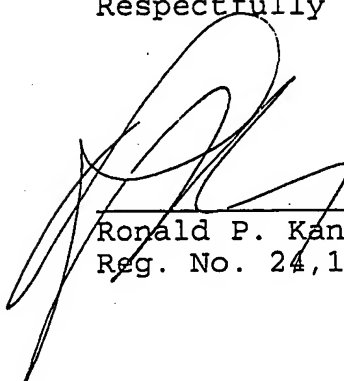
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If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the

overpayment to Deposit Account # 18-0013.

Respectfully submitted,

Date: February 13, 2004



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